Multirate 155 Mbps/622 Mbps/1244 Mbps/1250 Mbps Burst Mode Clock and Data Recovery IC with Deserializer

ADN2855

FEATURES

Serial data input
- **155.52 Mbps/622.08 Mbps/1244.16 Mbps/1250.00 Mbps**

12-bit acquisition time
4-bit parallel LVDS output interface
Patented dual-loop clock recovery architecture
Integrated PRBS generator
Byte rate reference clock
Loss-of-lock indicator
Supports double data rate (DDR)-compatible FPGA
I²C interface to access optional features
Single-supply operation: 3.3 V
Power
- **670 mW typical in serial output mode**
- **825 mW typical in deserializer mode**

5 mm × 5 mm, 32-lead LFCSP

APPLICATIONS

Passive optical networks
GPON/BPON/GEPON OLT receivers

GENERAL DESCRIPTION

The ADN2855 is a burst mode clock and data recovery IC designed for GPON/BPON/GEPON optical line terminal (OLT) receiver applications. The part can operate at 155.52 Mbps, 622.08 Mbps, 1244.16 Mbps, or 1250.00 Mbps data rates, selectable via the I²C interface.

The ADN2855 frequency locks to the OLT reference clock and aligns to the input data within 12 bits of the start of the preamble. The device provides a full rate or an optional half rate output clock for a double data rate (DDR) interface to an FPGA or digital ASIC.

All specifications are quoted for −40°C to +85°C ambient temperature, unless otherwise noted. The ADN2855 is available in a compact 5 mm × 5 mm, 32-lead chip scale package.

FUNCTIONAL BLOCK DIAGRAM

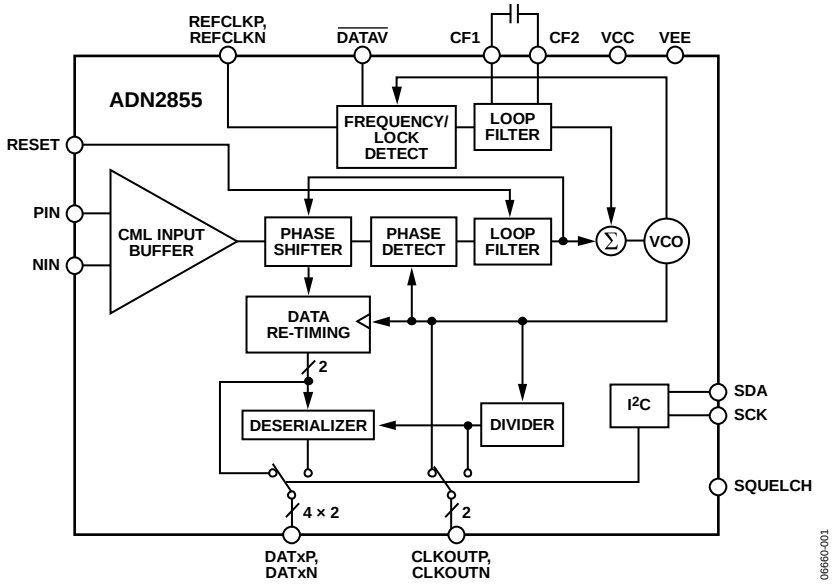

Figure 1.

Rev. 0

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REVISION HISTORY

1/09—Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, input data pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT BUFFER—DC CHARACTERISTICS					
Input Voltage Range	@ PIN or NIN, dc-coupled	VCC – 0.6		VCC – 0.1	V
Peak-to-Peak Differential Input	PIN – NIN	0.2		1.2	V
ACQUISITION TIME (BDR Mode[1])					
Lock to Preamble Data	1250.00 Mbps		12		Bits
	1244.16 Mbps		12		Bits
	622.08 Mbps		12		Bits
	155.52 Mbps		6		Bits
POWER SUPPLY VOLTAGE		3.0	3.3	3.6	V
POWER SUPPLY CURRENT	Serial output mode		204		mA
	Deserializer mode		250		mA
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] BDR mode = burst clock and data recovery mode, whereas CDR = continuous clock and data recovery mode.

JITTER SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, input data pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
PHASE-LOCKED LOOP CHARACTERISTICS					
Jitter Tolerance	1250.00 Mbps, $2^{23} - 1$ PRBS				
	50 kHz	3.0			UI p-p
	500 kHz	1.0			UI p-p
	10 MHz	0.5			UI p-p
	1244.16 Mbps, $2^{23} - 1$ PRBS				
	50 kHz	3.0			UI p-p
	500 kHz	1.0			UI p-p
	10 MHz	0.5			UI p-p
	622.08 Mbps, $2^{23} - 1$ PRBS				
	25 kHz	2.5			UI p-p
	250 kHz	1.0			UI p-p
	155.52 Mbps, $2^{23} - 1$ PRBS				
	6.5 kHz	3.5			UI p-p
	65 kHz	1.0			UI p-p

OUTPUT AND TIMING SPECIFICATIONS

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVDS OUPUT CHARACTERISTICS						
CLKOUTP/CLKOUTN, DATxP/DATxN						
Differential Output Swing	V_{DIFF}	See Figure 3	260	320	400	mV
Output High Voltage	V_{OH}				1475	mV
Output Low Voltage	V_{OL}		925			mV
Output Offset Voltage	V_{OS}		1125	1200	1275	mV
Output Impedance		Differential		100		Ω
LVDS Outputs Timing						
Rise Time		20% to 80%		115	220	ps
Fall Time		80% to 20%		115	220	ps
Setup Time	t_S		0.5 − 20%	0.5		UI
Hold Time	t_H		0.5 − 20%	0.5		UI
I^2C INTERFACE DC CHARACTERISTICS (SCK, SDA)		LVCMOS				
Input High Voltage	V_{IH}		0.7 VCC			V
Input Low Voltage	V_{IL}				0.3 VCC	V
Input Current		V_{IN} = 0.1 VCC or V_{IN} = 0.9 VCC	−10.0		+10.0	µA
Output Low Voltage	V_{OL}	I_{OL} = 3.0 mA			0.4	V
I^2C INTERFACE TIMING						
SCK Clock Frequency					400	kHz
SCK Pulse Width High	t_{HIGH}		600			ns
SCK Pulse Width Low	t_{LOW}		1300			ns
Start Condition Hold Time	$t_{HD;STA}$		600			ns
Start Condition Setup Time	$t_{SU;STA}$		600			ns
Data Setup Time	$t_{SU;DAT}$		100			ns
Data Hold Time	$t_{HD;DAT}$		300			ns
SCK and SDA Rise/Fall Time	t_R/t_F		20 + 0.1 Cb[1]		300	ns
Stop Condition Setup Time	$t_{SU;STO}$		600			ns
Bus Free Time between a Stop and a Start	t_{BUF}		1300			ns
REFCLK CHARACTERISTICS		At REFCLKP or REFCLKN				
Input Voltage Range	V_{IL}			0		V
	V_{IH}			VCC		V
Minimum Differential Input Drive				100		mV p-p
Reference Frequency			10	155.52	200	MHz
Required Accuracy				0		ppm
LVTTL DC INPUT CHARACTERISTICS (SQUELCH, SADDR[2:1], RESET)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN} = 2.4 V			5	µA
Input Low Current	I_{IL}	V_{IN} = 0.4 V	−5			µA
LVTTL DC OUTPUT CHARACTERISTICS ($\overline{\text{DATAV}}$)						
Output High Voltage	V_{OH}	I_{OH} = −2.0 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V

[1] Cb = total board capacitance of one bus line in picofarads (pF). If mixed with high speed class of I^2C devices, faster fall times are allowed.

TIMING CHARACTERISTCS

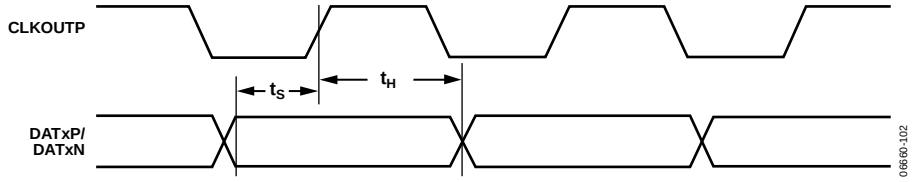


Figure 2. Output Timing

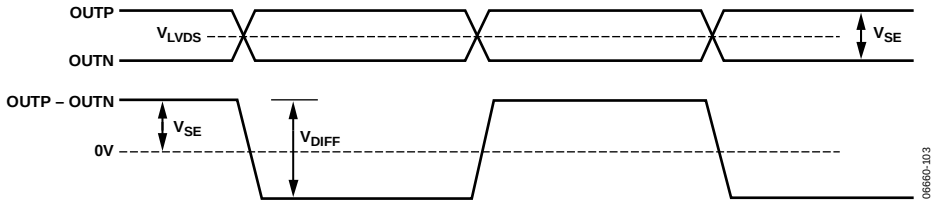


Figure 3. Single-Ended vs. Differential Output Specifications

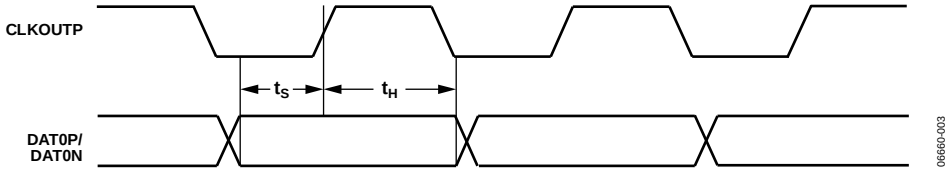


Figure 4. Serial Output Mode (Full Rate Clock)

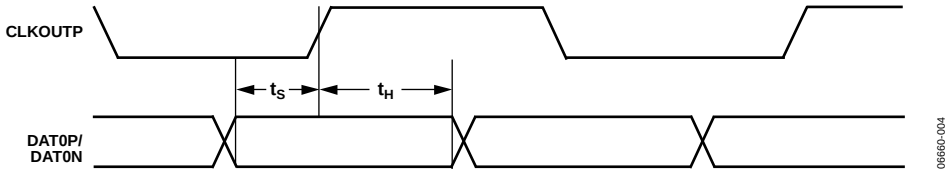


Figure 5. Serial Output Mode (Half Rate Clock, DDR Mode)

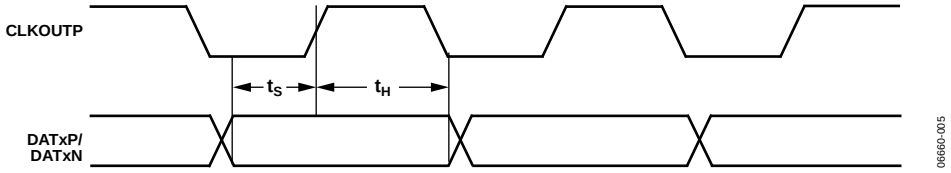


Figure 6. Nibble Output Mode (Full Rate Clock)

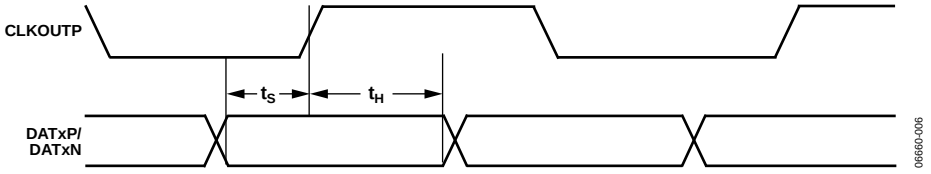


Figure 7. Nibble Output Mode (Half Rate Clock, DDR Mode)

RESET TIMING OPTIONS

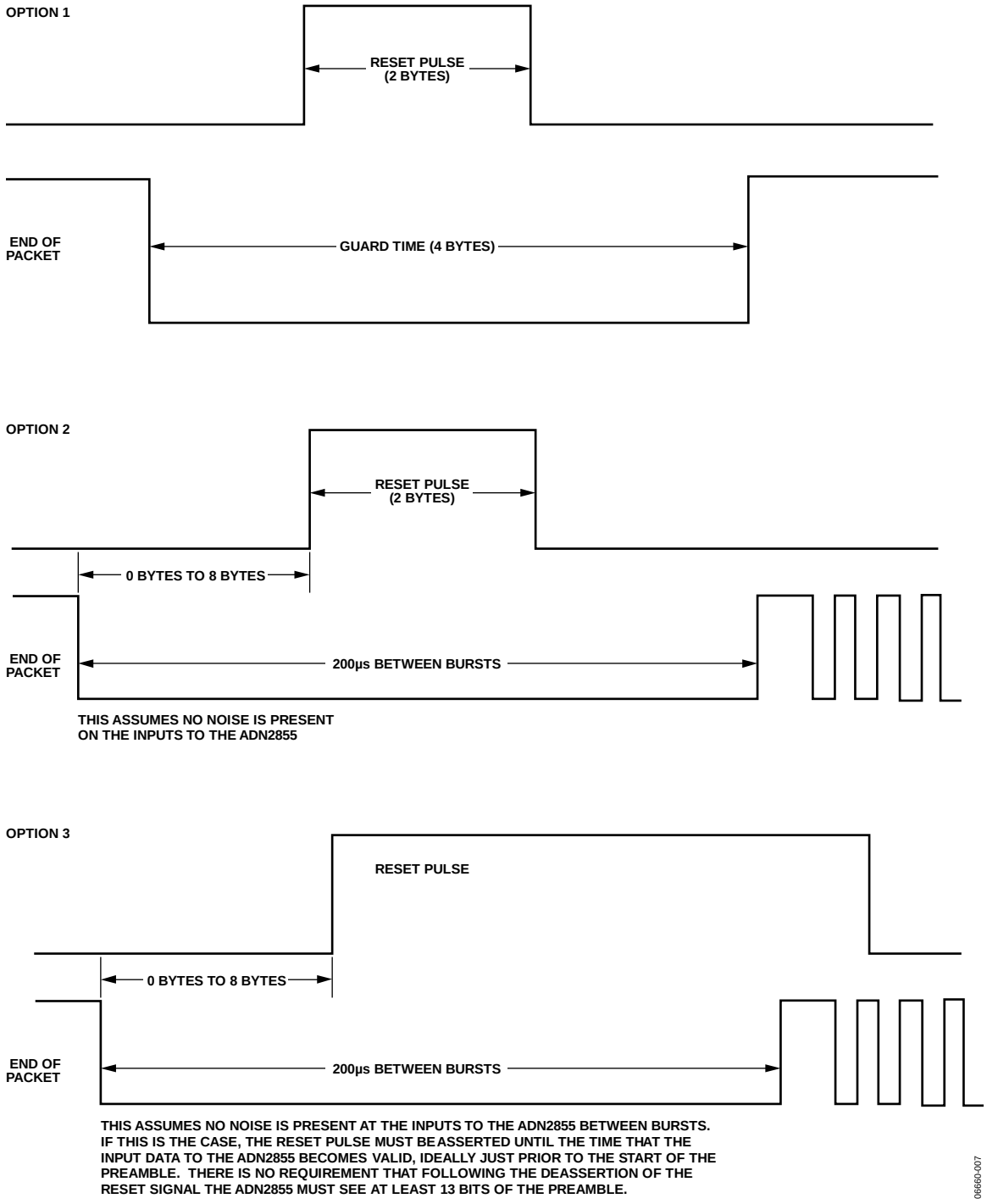


Figure 8. Reset Timing Options

ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, unless otherwise noted.

Table 4.

Parameter	Rating
Supply Voltage (VCC)	4.2 V
Minimum Input Voltage (All Inputs)	VEE − 0.4 V
Maximum Input Voltage (All Inputs)	VCC + 0.4 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for 4-layer board with exposed paddle soldered to VEE.

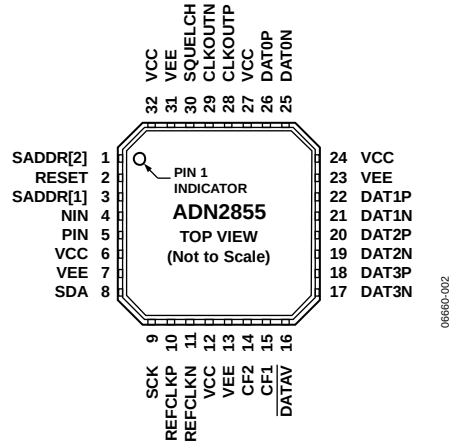
Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP (CP-32-3)	35.1	2.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THERE IS AN EXPOSED PAD ON THE BOTTOM OF THE PACKAGE THAT MUST BE CONNECTED TO VEE (GND).

Figure 9. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	SADDR[2]	DI	Slave Address Bit 2.
2	RESET	DI	RESET Pulse to be Asserted Prior to Incoming Burst. Active high.
3	SADDR[1]	DI	Slave Address Bit 1.
4	NIN	AI	Differential Data Input. CML.
5	PIN	AI	Differential Data Input. CML.
6	VCC	P	3.3 V Power.
7	VEE	P	GND.
8	SDA	IO	I^2C Data I/O.
9	SCK	DI	I^2C Clock.
10	REFCLKP	DI	Differential REFCLK Input.
11	REFCLKN	DI	Differential REFCLK Input.
12	VCC	P	3.3 V Power.
13	VEE	P	GND.
14	CF2	AO	Frequency Loop Capacitor.
15	CF1	AO	Frequency Loop Capacitor.
16	$\overline{\text{DATAV}}$	DO	Output Data Valid. LVTTL active low.
17	DAT3N	DO	Differential Deserialized Output MSB, LVDS.
18	DAT3P	DO	Differential Deserialized Output MSB, LVDS.
19	DAT2N	DO	Differential Deserialized Output Bit 2, LVDS.
20	DAT2P	DO	Differential Deserialized Output Bit 2, LVDS.
21	DAT1N	DO	Differential Deserialized Output Bit 1, LVDS.
22	DAT1P	DO	Differential Deserialized Output Bit 1, LVDS.
23	VEE	P	GND.
24	VCC	P	3.3 V Power.
25	DAT0N	DO	Differential Deserialized Output LSB, LVDS
26	DAT0P	DO	Differential Deserialized Output LSB, LVDS
27	VCC	P	3.3 V Power
28	CLKOUTP	DO	Differential Recovered Clock Output, LVDS.
29	CLKOUTN	DO	Differential Recovered Clock Output, LVDS.
30	SQUELCH	DI	Squelch Data and/or Clock Outputs. Active high.
31	VEE	P	GND
32	VCC	P	3.3 V Power.
33 (EPAD)	Exposed Pad (EPAD)	P	There is an exposed pad on the bottom of the package that must be connected to VEE (GND).

[1] P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output, IO = digital input/output.

I²C INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTION

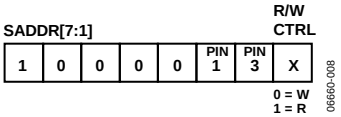


Figure 10. Slave Address Configuration

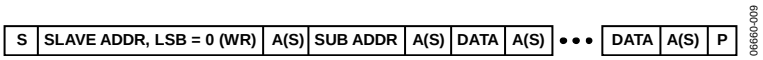


Figure 11. I²C Write Data Transfer

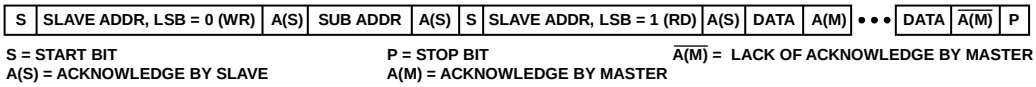


Figure 12. I²C Read Data Transfer

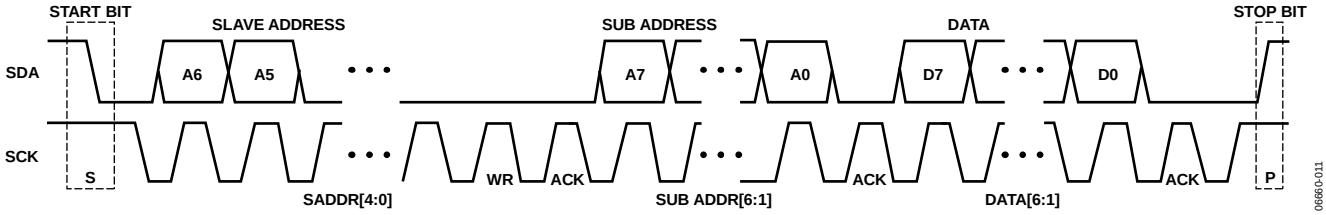


Figure 13. I²C Data Transfer Timing

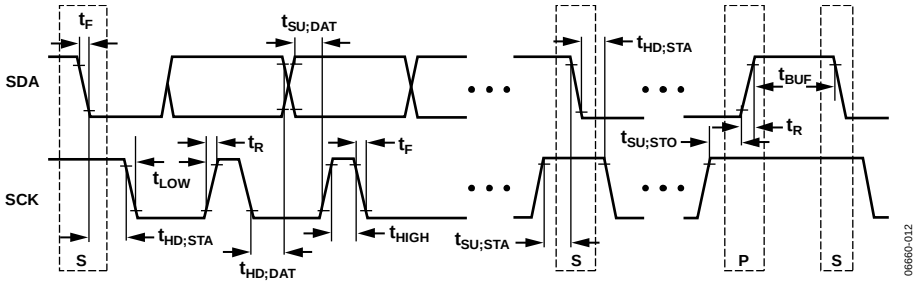


Figure 14. I²C Port Timing Diagram

Table 7. Internal Register Map[1]

Reg. Name	R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0
CTRLA	W	0x08	F_{REF} range		Data rate/DIV_F_{REF} ratio				0	Lock to REFCLK
CTRLA_RD	R	0x05	Readback CTRLA							
CTRLB	W	0x09	0	0	Initiate acquisition	0	0	0	0	0
CTRLB_RD	R	0x06	Readback CTRLB							
CTRLC	W	0x11	0	0	Bus swap	Parallel CLKOUT mode	RxCLK phase adjust		0	Output boost
CTRLD	W	0x22	Output mode	Disable data buffer	Disable clock buffer	0	0	0	0	Serial CLKOUT mode

[1] All writeable registers default to 0x00.

Table 8. Control Register, CTRLA[1]

Bit No.	Description
[7:6]	F_{REF} range 00 = 10 MHz to 25 MHz 01 = 25 MHz to 50 MHz 10 = 50 MHz to 100 MHz 11 = 100 MHz to 200 MHz
[5:2]	Data rate/DIV_F_{REF} ratio 0000 = 1 0001 = 2 0010 = 4 … n = 2^n … 1000 = 256
[1]	Set to 0
[0]	Lock to RFCLK 0 = lock to input data 1 = lock to reference clock

[1] Where DIV_F_{REF} is the divided down reference referred to the 10 MHz to 20 MHz band (see the Reference Clock section).

Table 9. Control Register, CTRLB

Bit No.	Description
[7:6]	Set to 0
[5]	Initiate acquisition; write a 1 followed by 0 to initiate a new acquisition
[4:0]	Set to 0

Table 10. Control Register, CTRLC

Bit No.	Description
[7:6]	Set to 0
[5]	Bus swap 0 = DAT3 is earliest bit 1 = DAT0 is earliest bit
[4]	Parallel CLKOUT mode 0 = full rate parallel clock 1 = half rate parallel clock (DDR mode)
[3:2]	RxCLK phase adjust 00 = CLK edge in center of eye 01 = +2 UI vs. baseline (CLK edge aligned with data transition) 10 = +0.5 UI vs. baseline 11 = −1.5 UI vs. baseline
[1]	Set to 0
[0]	Output boost 0 = default 1 = boost output swing

Table 11. Control Register, CTRLD

Bit No.	Description
[7]	Output mode 0 = parallel output 1 = serial output
[6]	Disable data buffer 0 = default 1 = disable data output buffer
[5]	Disable clock buffer 0 = default 1 = disable clock output buffer
[4:1]	Set to 0
[0]	Serial CLKOUT mode 0 = half rate serial clock 1 = full rate serial clock

THEORY OF OPERATION

The ADN2855 is designed specifically for burst mode data recovery in GPON/BPON/GEPON optical line terminal (OLT) receivers.

The ADN2855 requires a reference clock that is frequency locked to the incoming data. The FLL (frequency-locked loop) of the ADN2855 acquires frequency lock with respect to this reference clock, pulling the VCO towards 0 ppm frequency error. It is assumed that the upstream bursts to the OLT are clocked by the recovered clock from the optical network terminal (ONT) CDR. This guarantees frequency lock to the OLT system clock.

The ADN2855 has a preamble detector that looks for a maximum transition density pattern (1010…) within the preamble. Once this pattern is detected in the preamble, the on-chip delay/phase-locked loop (D/PLL) quickly acquires phase lock to the incoming burst within 12 UI of the 1010… pattern. The D/PLL also pulls in any remaining frequency error that was not pulled in by the FLL. The incoming data is retimed by the recovered clock and output either serially or in a 4-bit parallel output nibble.

The ADN2855 requires a RESET signal between bursts to set the device into a fast phase acquisition mode. The RESET signal must be asserted within 8 UI of the end of the previous burst, and it must be deasserted prior to the start of the maximum transition density portion of the preamble, which is specifically provided for the burst mode clock recovery device to acquire the phase of the incoming burst. The RESET signal must be at least 16 UI wide. See the Reset Timing Options section for more details.

FUNCTIONAL DESCRIPTION

FREQUENCY ACQUISITION

The ADN2855 operates in burst data recovery mode, which requires the use of the OLT system reference clock as an acquisition aid. The ADN2855 acquires frequency with respect to this reference clock, which is frequency locked to the incoming burst of data from the ONT.

The ADN2855 must be placed in lock to reference clock mode by setting CTRLA[0] = 1. A frequency acquisition is then initiated by writing a 1 to 0 transition into CTRLB[5]. This must be done well before the ADN2855 is expected to lock to an incoming burst, preferably right after power-up and once there is a valid reference clock being supplied to the device. As long as the reference clock to the ADN2855 is always present, this frequency acquisition needs to take place only once. It does not need to be repeated between bursts of data in its normal operating mode. The initial frequency acquisition with respect to the reference clock takes ~10 ms.

To lock to burst data, a RESET signal must be asserted following a previous burst (or at startup) according to the timing diagrams shown in the Reset Timing Options section. The RESET signal must be deasserted prior to the 1010… portion of the preamble. The ADN2855 uses a preamble detector that identifies the 1010… portion of the preamble and quickly acquires the phase of the incoming burst within 12 UI.

The frequency loop requires a single external capacitor between Pin 14, CF2, and Pin 15, CF1. A 0.47 µF ± 20%, X7R ceramic chip capacitor with <10 nA leakage current is recommended. Leakage current of the capacitor can be calculated by dividing the maximum voltage across the 0.47 µF capacitor, ~3 V, by the insulation resistance of the capacitor. The insulation resistance of the 0.47 µF capacitor should be greater than 300 MΩ.

$\overline{\text{DATAV}}$ Operation

The ADN2855 has a data valid indicator that asserts when the ADN2855 acquires the phase of the maximum transition density portion of the preamble. This takes 12 UI from the start of the 1010… pattern in the preamble. The $\overline{\text{DATAV}}$ output remains asserted until the RESET signal is asserted following the end of the current burst of data, at which point the $\overline{\text{DATAV}}$ output deasserts. The $\overline{\text{DATAV}}$ output is active low and is LVTTL compatible.

SQUELCH MODE

When the squelch input, Pin 30, is driven to a TTL high state, both the clock and data outputs are set to the zero state to suppress downstream processing. If the squelch function is not required, Pin 30 should be tied to VEE.

If it is desired that the DATxP/DATxN and CLKOUTP/CLKOUN outputs be squelched while the output data is invalid, then the $\overline{\text{DATAV}}$ pin can be hardwired directly to the SQUELCH input.

I²C INTERFACE

The ADN2855 supports a 2-wire, I²C-compatible serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any devices connected to the bus. Each slave device is recognized by a unique address. The ADN2855 has four possible 7-bit slave addresses for both read and write operations. The MSB of the 7-bit slave address, SADDR[7] is factory programmed to 1. Bit 2 of the slave address, SADDR[2], is set by Pin 1. Bit 1 of the slave address, SADDR[1], is set by Pin 3. Slave Address Bits[6:3] are defaulted to all 0s. The slave address consists of the seven MSBs of an 8-bit word. The LSB of the word, SADDR[0], sets either a read or write operation (see Figure 10). Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

To control the device on the bus, use the following protocol. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCK lines waiting for the start condition and correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADN2855 acts as a standard slave device on the bus. The data on the SDA pin is eight bits long supporting the 7-bit addresses plus the R/W bit. The ADN2855 has six subaddresses to enable the user-accessible internal registers (see Table 7 through Table 11). It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. Autoincrement mode is supported, allowing data to be read from or written to the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCK high period, the user should issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADN2855 does not issue an acknowledge, and returns to the idle condition. If the

user exceeds the highest subaddress while reading back in autoincrement mode, then the highest subaddress register contents continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. In a no-acknowledge condition, the SDATA line is not pulled low on the ninth pulse. See Figure 11 and Figure 12 for sample write and read data transfers and Figure 13 for a more detailed timing diagram.

REFERENCE CLOCK

A reference clock is required to perform burst mode clock and data recovery with the ADN2855. The reference clock must be frequency locked to the incoming burst data. It is assumed that the incoming burst data from the ONT is timed by a clock recovered from the downstream data from the OLT and, therefore, is inherently frequency clocked to the OLT system clock. The reference clock can be driven differentially or single-ended. See Figure 15 and Figure 16 for sample configurations.

The REFCLK input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (for example, LVPECL or LVDS) or a standard single-ended low voltage TTL input, providing maximum system flexibility. Phase noise and duty cycle of the reference clock are not critical.

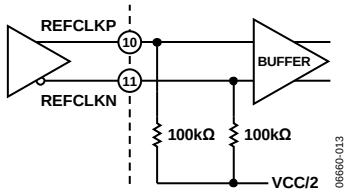


Figure 15. Differential REFCLK Configuration

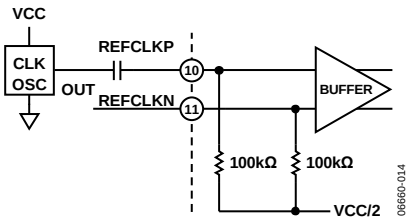


Figure 16. Single-Ended REFCLK Configuration

The ADN2855 must be operated in lock to reference clock mode when in burst data recovery mode. Lock to reference clock mode is enabled by writing a 1 to I²C Control Register CTRLA, Bit 0. A frequency acquisition in this mode must be initiated by writing a 1 to 0 transition to CTRLB[5].

Using the Reference Clock to Lock onto Data

In this mode, the ADN2855 locks onto a frequency derived from the reference clock according to the following equation:

$$Data\ Rate/2^{CTRLA[5:2]} = REFCLK/2^{CTRLA[7:6]}$$

The user must know exactly what the data rate is and provide a reference clock that is a function of this rate. The reference clock can be anywhere between 10 MHz and 200 MHz. By default, the ADN2855 expects a reference clock of between 10 MHz and 25 MHz. If it is between 25 MHz and 50 MHz, 50 MHz and 100 MHz, or 100 MHz and 200 MHz, the user needs to configure the ADN2855 to use the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7:6].

Table 12. CTRLA Settings

Bit No.	Description
CTRLA[7:6]	F_{REF} range 00 = 10 MHz to 25 MHz 01 = 25 MHz to 50 MHz 10 = 50 MHz to 100 MHz 11 = 100 MHz to 200 MHz
CTRLA[5:2]	Data rate/DIV_F_{REF} ratio 0000 = 1 0001 = 2 … n = 2^n … 1000 = 256

The user can specify a fixed integer multiple of the reference clock to lock onto using CTRLA[5:2], where CTRLA should be set to the data rate/DIV_F_{REF} ratio, where DIV_F_{REF} represents the divided-down reference referred to the 10 MHz to 25 MHz band. For example, if the reference clock frequency is 38.88 MHz and the input data rate is 622.08 Mbps, then CTRLA[7:6] should be set to 01 to give a divided-down reference clock of 19.44 MHz. CTRLA[5:2] should be set to 0101, that is, 5, because

$$622.08\ Mbps/19.44\ MHz = 2^5$$

While the ADN2855 is operating in lock to reference clock mode, if the user ever changes the reference frequency, the F_{REF} range (CTRLA[7:6]), or the data rate/DIV_F_{REF} ratio (CTRLA[5:2]), this must be followed by writing a 0 to 1 transition into the CTRLB[5] bit to initiate a new frequency acquisition.

OUTPUT MODES

Parallel or Serial Output Mode

The output of the ADN2855 can be configured in a 4-bit parallel output nibble mode, or it can be configured in a serial output mode. The default mode of operation is for the Rx data to be deserialized and output in a 4-bit nibble, present at DATxP/DATxN, where the earliest bit is present on DAT3P/DAT3N. Setting Bit CTRLC[5] = 1 reverses the order of the DATxP/DATxN bus such that the earliest bit is present on DAT0P/DAT0N.

Setting bit CTRLD[7] = 1 puts the device into serial output mode. In this mode, the Rx data is present on DAT0P/DAT0N.

Double Data Rate Mode

The default output mode for the ADN2855 is for a 4-bit deserialized output with a full rate output clock, where the output data switches on the rising edge of the output clock. When the ADN2855 is programmed to be in parallel output mode (CTRLD[7] = 0), setting CTRLC[4] = 1 puts the ADN2855 clock output through divide-by-two circuitry, allowing direct interfacing to FPGAs that support data clocking on both rising and falling edges.

When the ADN2855 is in serial output mode (deserializer off), CTRLD[7] = 1, the default is for a half rate output clock where the data switches on both falling and rising edges of the output clock. Setting CTRLD[0] = 1 sets the serial clock output into full rate mode so that the output data switches only on the rising edges of the output clock.

RxCLK Phase Adjust

The ADN2855 provides the option of adjusting the phase of the output clock with respect to the parallel output data. In parallel mode, the duration of each bit is 4 UI wide, due to the deserialization. There are three additional phase adjust options other than the baseline (that is, CLK edge in the center of the data eye): +2 UI, +0.5 UI, and −1.5 UI. The output clock phase adjustment feature is accessed via CTRLC[3:2]. See Table 10 for details.

DISABLE OUTPUT BUFFERS

The ADN2855 provides the option of disabling the output buffers for power savings. The clock output buffers can be disabled by setting CTRLD[5] = 1. For additional power savings (for example, in a low power standby mode), the data output buffers can also be disabled by setting CTRLD[6] = 1.

APPLICATIONS INFORMATION

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance. The exposed pad should be connected to the GND plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a 10 µF electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. When using 0.1 µF and 1 nF ceramic chip capacitors, they should be placed between the IC power supply VCC and VEE, as close as possible to the ADN2855 VCC pins.

If connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance. Refer to the schematic in Figure 17 for recommended connections.

By using adjacent power supply and GND planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{PLANE}[\text{pf}] = 0.88\varepsilon_r A/d$$

where:
ε_r is the dielectric constant of the PCB material.
A is the area of the overlap of power and GND planes (cm^2).
d is the separation between planes (mm).

For FR-4, ε_r = 4.4 mm and 0.25 mm spacing, $C_{PLANE} \approx 15$ pF/cm^2.

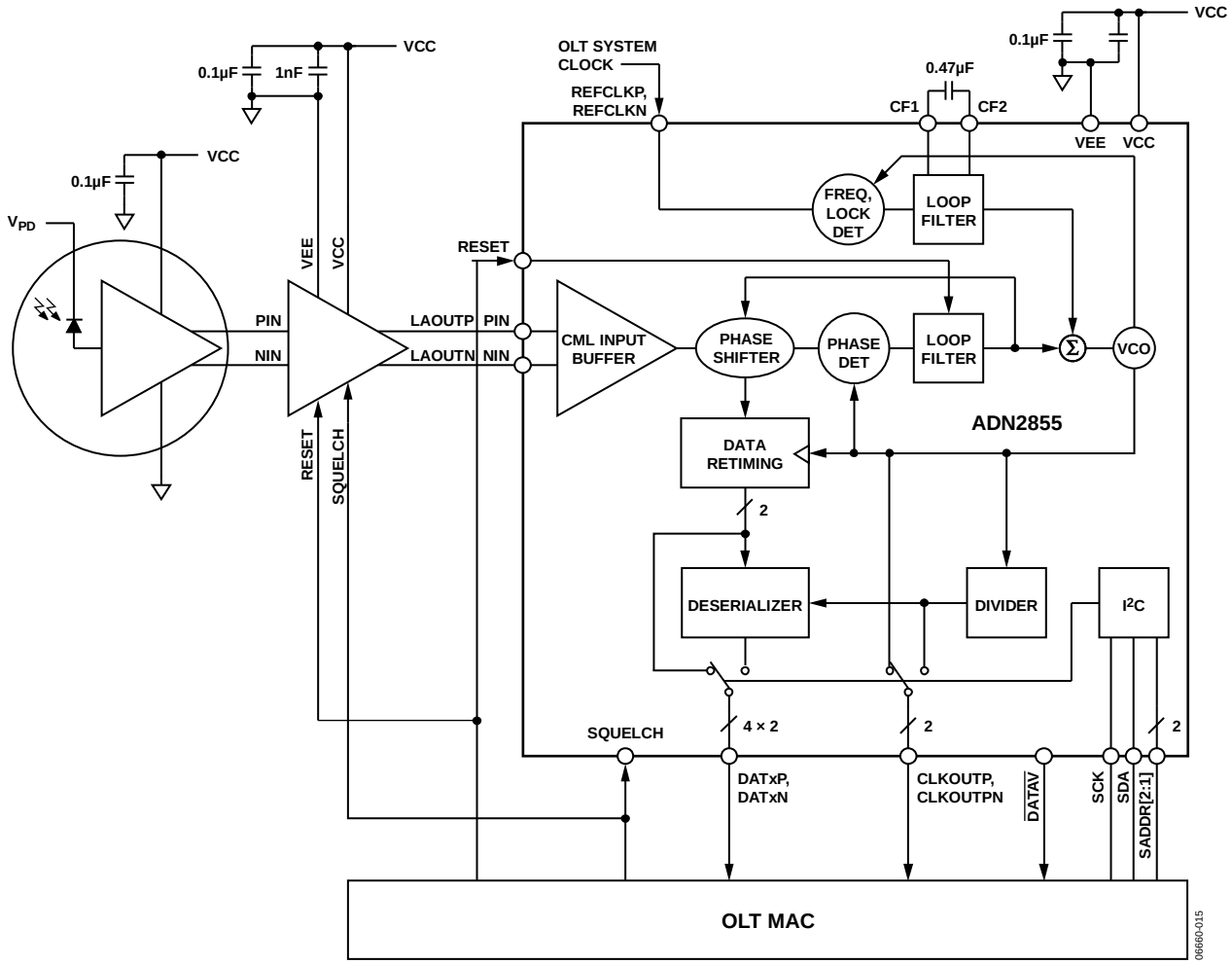


Figure 17. Typical Application Circuit

Transmission Lines

Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections: PIN, NIN, CLKOUTP, CLKOUTN, DATxP, DATxN (also REFCLKP and REFCLKN if a high frequency reference clock is used, such as 155.52 MHz). It is also necessary for the PIN/NIN input traces to be matched in length, and the CLKOUTP/CLKOUTN and DATxP/DATxN output traces to be matched in length to avoid skew between the differential traces. All high speed LVDS outputs, CLKOUTP/CLKOUTN and DATxP/DATxN, require a 100 Ω differential termination at the differential input to the device being driven by the ADN2855 outputs.

The high speed inputs, PIN and NIN, are internally terminated with 50 Ω to an internal reference voltage.

As with any high speed mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

Soldering Guidelines for Chip Scale Package

The lands on the 32-lead LFCSP are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad to ensure that the solder joint size is maximized. Visit www.analog.com/CP-32-3 for further details. The bottom of the chip scale package has a central exposed pad. The pad on the PCB should be at least as large as this exposed pad. The user must connect the exposed pad to VEE (GND) using plugged vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

OUTLINE DIMENSIONS

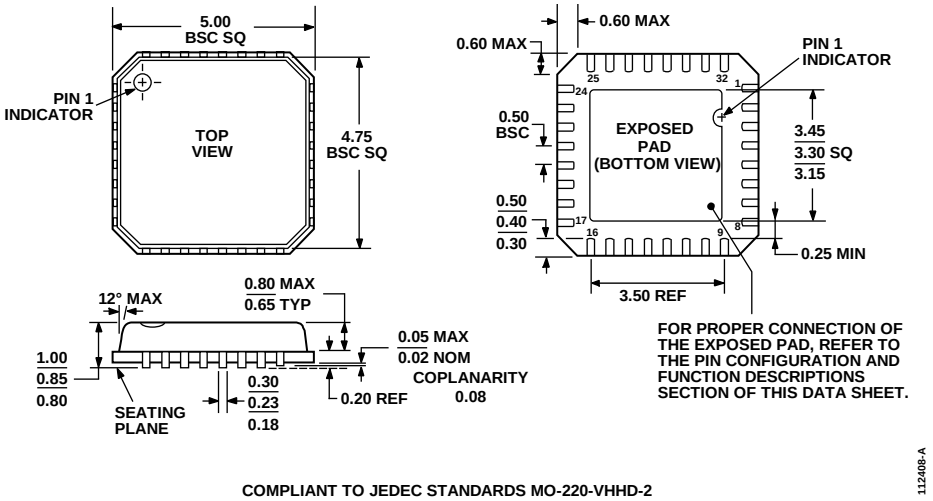


Figure 18. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN2855ACPZ[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
ADN2855ACPZ-R7[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
ADN2855-EVALZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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